Unity ECC: Unified Memory Protection Against Bit and Chip Errors

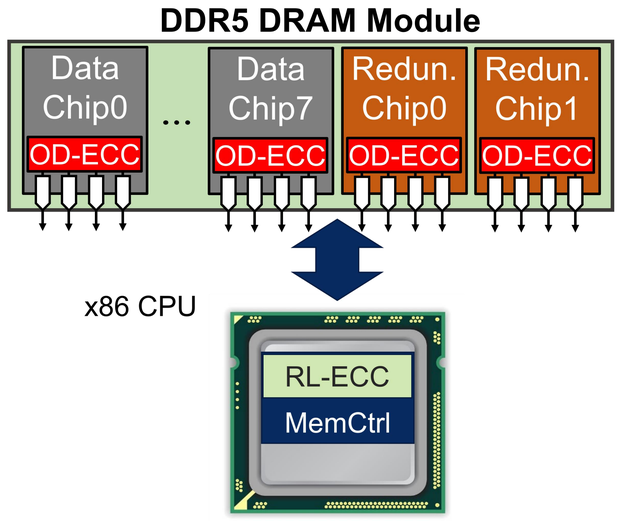
Dongwhee Kim[†], Jaeyoon Lee[†], Wonyeong Jung[†], Michael B. Sullivan[††], and Jungrae Kim[†]
[†]Sungkyunkwan University, [††]NVIDIA Corporation

Abstract

DRAM vendors utilize On-Die Error Correction Codes (OD-ECC) to correct random bit errors internally. Meanwhile, system companies utilize Rank-Level ECC (RL-ECC) to protect data against chip errors. Separate protection increases the redundancy ratio to 32.8% in DDR5 and incurs significant performance penalties. This paper proposes a novel RL-ECC, Unity ECC, that can correct both single-chip and double-bit error patterns. Unity ECC corrects double-bit errors using unused syndromes of single-chip correction. Our evaluation shows that Unity ECC without OD-ECC can provide the same reliability level as Chipkill RL-ECC with OD-ECC. Moreover, it can significantly improve system performance and reduce DRAM energy and area by eliminating OD-ECC.

Introduction

Motivation



1. DDR5's two-level ECC (OD-ECC + RL-ECC) leads to a 32.8% redundancy ratio.
2. OD-ECC in DDR5 increases performance overhead, energy use, and chip area.
3. RL-ECC in DDR5 has many unused syndromes, solely for error detection.

Goal

Removing OD-ECC overheads while maintaining reliability levels against bit and chip errors.

Key Idea

Eliminate OD-ECC and remap unused syndromes in RL-ECC.

Unity ECC

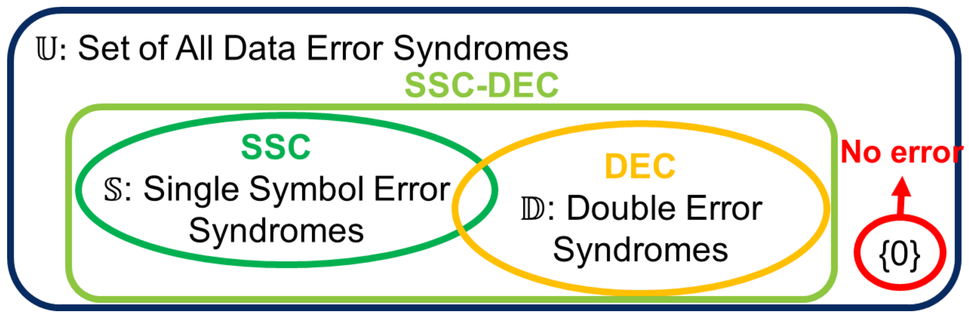
Summary

1. Unity ECC is a single-level RL-ECC (also Chipkill).
2. Unity ECC can correct single chip and double bit errors.
3. Unity ECC has SSC-DEC (Single Symbol Correction-Double Error Correction) capabilities.

ECC-ExerSim

✓ ECC-Exercise and Simulator
✓ Github open source
✓ Objective: Reliability evaluation
✓ CERN-OHL-S-2.0 license

H-matrix Properties (Syndrome Remapping)



1. **All columns are non-zero**.
2. **DEC**: The sums (XOR operation) of any two columns are unique non-zero values.
3. **SSC**: The sums (XOR operation) of all symbol-aligned columns are unique non-zero values.
4. **SSC-DEC**: All sums from properties 2 and 3 should be unique.

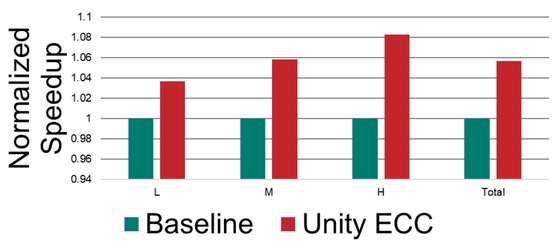
H-matrix example of (10, 8) Unity ECC

$$H = \begin{bmatrix} \alpha^{25} & \alpha^{39} & \alpha^{63} & \alpha^{108} & \alpha^{141} & \alpha^{184} & \alpha^{215} & \alpha^{230} & \alpha^{0} & 0 \\ \alpha^{50} & \alpha^{78} & \alpha^{126} & \alpha^{216} & \alpha^{27} & \alpha^{113} & \alpha^{175} & \alpha^{205} & 0 & \alpha^{0} \end{bmatrix}$$

Construct the H-matrix based on Reed-Solomon code. Unity ECC is flexible, allowing adjustments to codeword and data lengths, making it applicable to various systems.

Evaluation

Performance & DRAM energy consumption



✓ Baseline: OD-ECC + RL-ECC
✓ Unity ECC: RL-ECC
✓ L: Low memory intensity mix
✓ M: Medium memory intensity mix
✓ H: High memory intensity mix

Unity ECC can speed up 4-core execution by **8.2%** (“H” mix) and improve DRAM energy consumption by **8.0%** using SPEC CPU 2006 benchmarks.

Reliability

Unity ECC maintains reliability levels against bit and chip errors.

Hardware Overheads

Unity ECC can decrease DRAM chip size by **6.9%**.

Conclusion

This paper presents Unity ECC, a novel memory protection scheme that addresses key challenges in DRAM technology: high access latencies, energy consumption, hardware overhead, and susceptibility to vulnerabilities. Implemented for DDR5 DRAM as a single-tier RL-ECC, Unity ECC eliminates OD-ECC and reduces DRAM redundancy from 32.8% to 25%, leading to improved performance and reduced energy consumption. The proposed flexible algorithm and efficient decoding method allow Unity ECC to offer significant benefits over conventional DDR5 while maintaining acceptable levels of system reliability.

SUNG KYUN KWAN UNIVERSITY(SKKU)

SC23 Denver, CO | i am hpc.